

High-Performance High- κ /Metal Gates for 45nm CMOS and Beyond with Gate-First Processing

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Abstract

Gate-first integration of band-edge (BE) high- κ /metal gate nFET devices with dual stress liners and silicon-on-insulator substrates for the 45nm node and beyond is presented. We show the first reported demonstration of improved short channel control with high- κ /metal gates (HK/MG) enabled by the thinnest T_{inv} (<12Å) for BE nFET devices to-date, consistent with simulations showing the need for <14Å T_{inv} at L_{gate} <35nm. We report the highest BE HK/MG nFET I_{dsat} values at 1.0V operation. We also show for the first time BE high- κ /metal gate pFET's fabricated with gate-first high thermal budget processing with thin T_{inv} (<13Å) and low V_t s appropriate for pFET devices. The reliability in these devices was found to be consistent with technology requirements. Integration of high- κ /metal gate nFET's into CMOS devices yielded large SRAM arrays.

Introduction

Scaling the channel length at the 45nm node and beyond has significant performance impact both from intrinsic device and extrinsic improvements [1]. Simulations in Fig. 1 and Fig. 2 show that high performance logic requires dual work-function devices near 110mV to the band-edge (BE) values of silicon and T_{inv} <14Å to show appreciable performance and short channel benefit over SiON/Poly-Si devices. Many reports exist detailing the thermal instabilities of the high- κ /metal (HK/MG) devices as a remaining roadblock to the implementation of dual work-function HK/MG in high-performance CMOS in gate-first processing, in particular the pFET [2,3]. These thermal instabilities lead to threshold voltage shifts and re-growth [4,5] in the gate stack which has prevented the implementation of HK/MG using gate-first processing. The majority of the reported near-BE HK/MG nFET/pFET solutions implement a damascene integration approach which suffers from high overlap capacitance (C_{ov}) due to the high- κ material along the spacer sidewall degrading AC performance and reduced mobility due to restricted thermal budgets [6]. This work focuses on utilizing a gate-first approach to overcome these limitations.

Device Fabrication and Results

Short channel HK/MG devices were fabricated from <20Å HfO₂ with thermally stable BE metal gates in a gate-first approach where conventional poly-Si is deposited over the metal gates. Following a lithographic patterning and gate stack etch process, a conventional self-aligned implant process flow with a final S/D spike RTA ($T > 1080^\circ\text{C}$) + advanced annealing (AA) and dual stress liner (DSL) with conventional MOL and BEOL was used. Fig. 3 shows a TEM image of the nFET HK/MG stack after full build showing a physical gate length of 33nm. Short channel device properties of the HK/MG nFET devices exhibit superior drive current and short channel control as compared to state-of-the-art 65nm node 11Å SiON/Poly-Si gate stacks. DIBL improvement of 15mV at fixed L_{gate} as shown in Fig. 4 supports a 5nm reduction in channel length as predicted from the simulations in Fig 1. The improved short channel control is due to high- κ /metal gate process improvements that enable T_{inv} <12Å as seen in Fig 5 by preventing re-growth that plagues gate-first processing. Fig. 6 shows a DC I_{dsat} of 1240uA/um @ $I_{off} = 200\text{nA/um}$ with a corresponding AC I_{dsat} 1364uA/um (non-self-heated) in the nFET HK/MG devices at 1.0V. Well controlled V_{tlin} / V_{tsat} roll-off to an L_{gate} of 25nm is shown in Fig. 7, demonstrating excellent short channel control. Fig. 8 shows that I_{dsat} is maintained as L_{gate} is scaled compared to an 11Å SiON at fixed I_{off} and optimal C_{ov} . The flatness of the HK/MG vs. SiON curve again demonstrates the improved short channel control in these HK/MG

devices. These stacks are compatible with existing stress adders as shown in Fig 9. There is a 15% change in R_{on} [7] at a L_{gate} of 35nm with a stressed liner which results in the expected drive current improvement.

HK/MG pFET stacks fabricated using high work-function metals (ϕ_m) in a gate-first integration scheme suffer from two problems: (a) >500 meV lower effective ϕ_m on HfO₂ [2,3] and (b) significant interfacial layer re-growth [5]. The problem is highlighted in Fig. 10 which shows that aggressive stacks ($T_{inv}=14\text{\AA}$) have V_t s which are at least 500mV away from pFET BE. These pFET problems can be circumvented and the initially high V_t can be lowered by 720mV by process optimization resulting in a pFET V_t @ BE while simultaneously maintaining aggressive T_{inv} (<13Å) & high mobility (92% of universal) for BE pFET HK/MG stacks fabricated in a gate-first process as shown in Figs. 11, 12 and 13. The simulations in Fig. 2 show that pFETs and nFETs with T_{inv} <14Å and ϕ_m <110 mV from BE improve performance in RO delay compared to SiON/Poly-Si.

Reliability Results

The reliability of the HK/MG gate devices was evaluated for TDDB, hot carrier, PBTi and NBTi. The charge trapping characteristics were measured at elevated temperature and voltages for lifetime predictions using a stretched exponential model [8]. The predicted 10yr PBTi shift in Fig. 14 is shown to be acceptable. The hot carrier degradation in the BE HK/MG nFETs is consistent with models for SiON/Poly-Si nFETs. The model projection to use condition was below target with V_{eff} corrected for self-heating effects, demonstrating that hot carrier degradation is acceptable. Breakdown was confirmed to be non-progressive for metal gates. The voltage acceleration power-law exponent is superior for HfO₂ compared to SiON due the steeper current/voltage dependence in high- κ versus SiON and the area scaling Weibull slope is better than for SiON in 65nm technology (Fig. 15). The BE HK/MG pFETs threshold voltage stability under negative bias stress (Fig. 16) follows a power law and is projected to be consistent with technology needs [8].

SRAM Results

Manufacturability studies of HK/MG integrated using a gate-first approach were performed in a 300mm production line to evaluate the yield. In this study high-performance nFET BE HK/MG devices were first integrated with SiON/Poly-Si pFET's to form large SRAM arrays. The top-down SEM image in Fig. 17 shows a portion of a large SRAM device array fabricated with HK/MG nFET's and SiON/Poly-Si pFET's. Fig. 18 shows the operating window of the SRAM array containing HK/MG devices at different array (Varray) and BL/logic (Vdd BL) voltages, demonstrating that good V_{ddmin} and V_{ddmax} values are obtained.

Conclusions

By using an integration method that is consistent with traditional high thermal budget gate-first CMOS processing we have demonstrated improved short channel control with high- κ /metal gate devices compared to SiON. The aggressive T_{inv} scaling enables L_{gate} scaling and results in the highest performing HK/MG nFET devices to-date for the 45nm technology and beyond. BE pFET HK/MG devices are shown with the lowest T_{inv} to-date providing a gate-first integration path for dual BE HK/MG CMOS technology implementation. Manufacturability evaluations of the nFET high- κ /metal gate devices with performance adders successfully yielded large SRAM arrays.

References

[1] J. Sleight et al., International Electron Devices Meeting (IEDM), San Fran., CA, 2006 [2] E. Cartier et al., 2005 Symposium on VLSI Technology, pp. 230-1, 2005 [3] J. K. Schaeffer et al., APL, 85, pg. 1826, 2004 [4] F. Andrieu et al. International Electron Devices Meeting (IEDM), San Fran., CA, 2006 [5] E. Gusev, V. Narayanan, M. Frank, IBM J. Res. & Dev. Vol. 50 (4-5) pp. 387-410 Jul-Sep. 2006 [6] V. Narayanan et al., IEEE Elec. Dev. Lett. Vol.27 (7) pp. 591-4, July 2006 [7] K. Rim et al., IEDM Technical Digest, pp. 43-6, 2002 [8] S. Zafar et al., VLSI Technology Digest, pp. 30-21, 2006

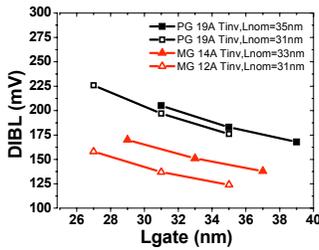


Figure 1: Simulations showing DIBL response for HK/MG and SiON/Poly-Si devices as a function of Lgates at various Tinv values.

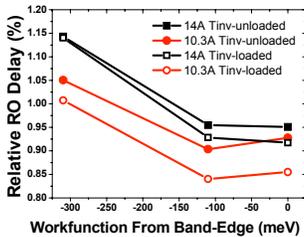


Figure 2: Simulations showing relative RO delay vs. workfunction from BE for HK/MG.

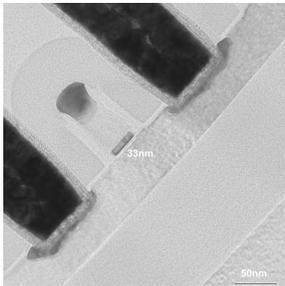


Figure 3: TEM image of the HK/MG nFET at 33nm Lgate.

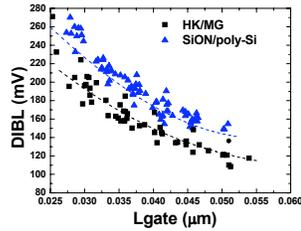


Figure 4: DIBL vs. Lgate for HK/MG vs. SiON/Poly-Si nFETs.

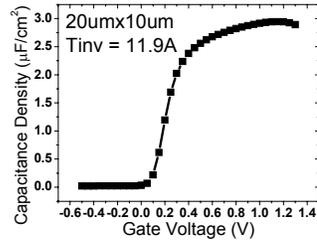


Figure 5: C-V Plot for the BE HK/MG nFET gate stack.

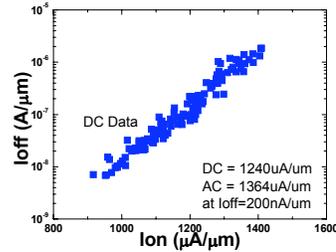


Figure 6: Ion vs. Ioff plot of HK/MG nFETs.

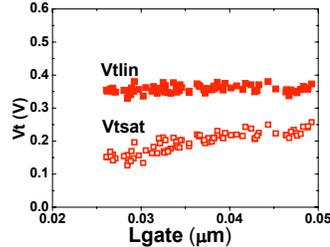


Figure 7: Vt roll off for BE HK/MG nFETs.

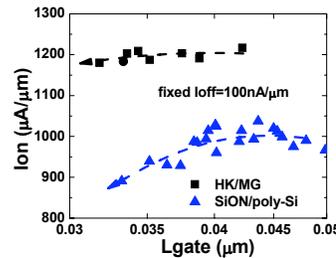


Figure 8: Ion roll-off plot comparing HK/MG and SiON/Poly-Si nFETs devices.

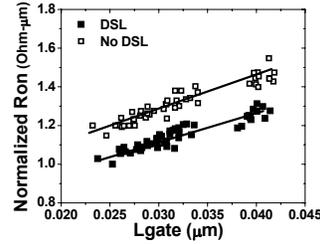


Figure 9: Normalized Ron vs. Lgate in HK/MG nFETs w/ and w/o DSL.

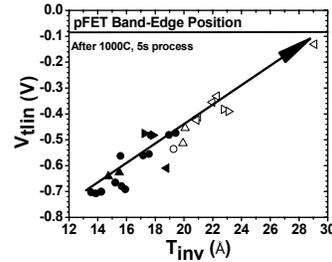


Figure 10: Universal pFET Vt vs. Tinv curve for multiple HfO₂/metal stacks after 1000C/5sec.

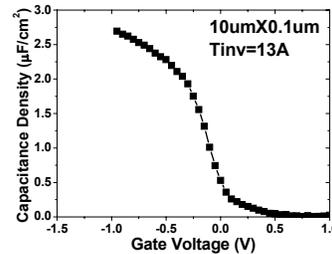


Figure 11: C-V Plot of HK/MG pFET device.

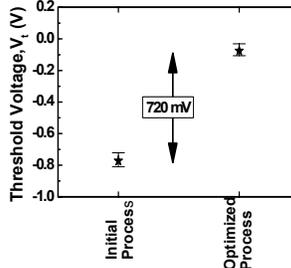


Figure 12: Vt plot for optimized BE HK/MG pFETs.

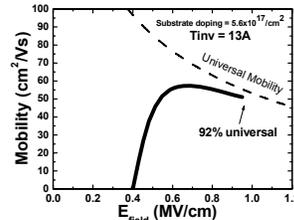


Figure 13: Mobility vs. inversion charge for the HK/MG pFET gate stack.

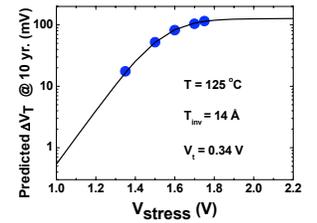


Figure 14: PBTI response of the HK/MG nFETs.

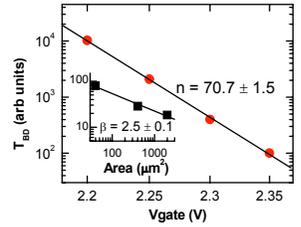


Figure 15: TDDB voltage acceleration and Weibull slope for band-edge HK/MG nFETs.

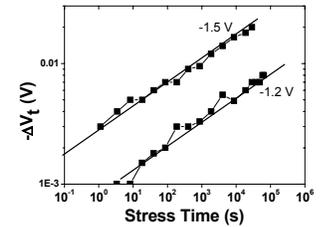


Figure 16: NBTI response for the BE HK/MG pFETs.

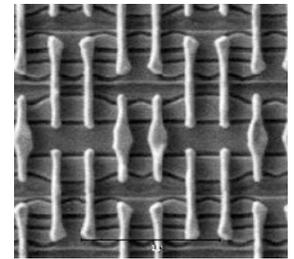


Figure 17: Top-down SEM of the large SRAM array w/ BE HK/MG nFETs & SiON/Poly-Si pFETs.

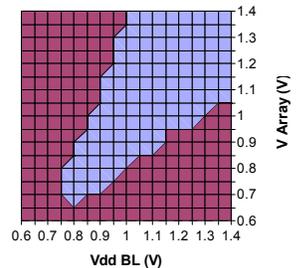


Figure 18: Shmoo plot of a large SRAM array with HK/MG nFETs (light zone is zero fails).